AMENDMENTS IN THE CLAIMS

1. (currently amended) In a[[n]] multiprocessor data processing system (MP) ~~configured according to IA-32 architecture~~, a method for dynamically providing spare processor resources when an operating processor fails, said method comprising:

holding-off a spare processor during an initial POST (power on self test), wherein said spare processor is available within said MP along with at least two operating processors, and said spare processor is not allocated any processing load by the operating system (OS) following the POST; and

when one of the operating processors is determined to be failing, dynamically activating said spare processor to replace the failing operating processor, wherein the processing load of the failing processor is automatically sent to the spare processor for processing.

2. (currently amended) The method of Claim 1, wherein:

said MP includes a basic input/output system (BIOS) and a processor register linked to said BIOS, which indicates which processors among said operating processors and said spare processors are currently available to said OS for allocating load; and[[,]]

~~wherein~~ said holding off of the spare processor comprises:

setting a bit within said processor register to a first value corresponding to assigning each of said operating processors to an active state during said initial POST, wherein said active state indicates to said OS that the corresponding operating processor is available for allocating load; and

setting a next bit within the processor register to a second value corresponding to assigning said spare processor to an inactive state.

3. (currently amended) The method of Claim 2, wherein said dynamically activating step comprises:

re-setting a bit corresponding to the failing processor to an inactive state; and

setting said next bit corresponding to said spare processor to the first value indicating an active state.

4. (original) The method of Claim 1, wherein said holding off step comprises:

placing said spare processor in a low-power, standby state during system boot utilizing advanced configuration and power interface (ACPI) of the BIOS; and

subsequently handing off control of said MP from said BIOS to the OS